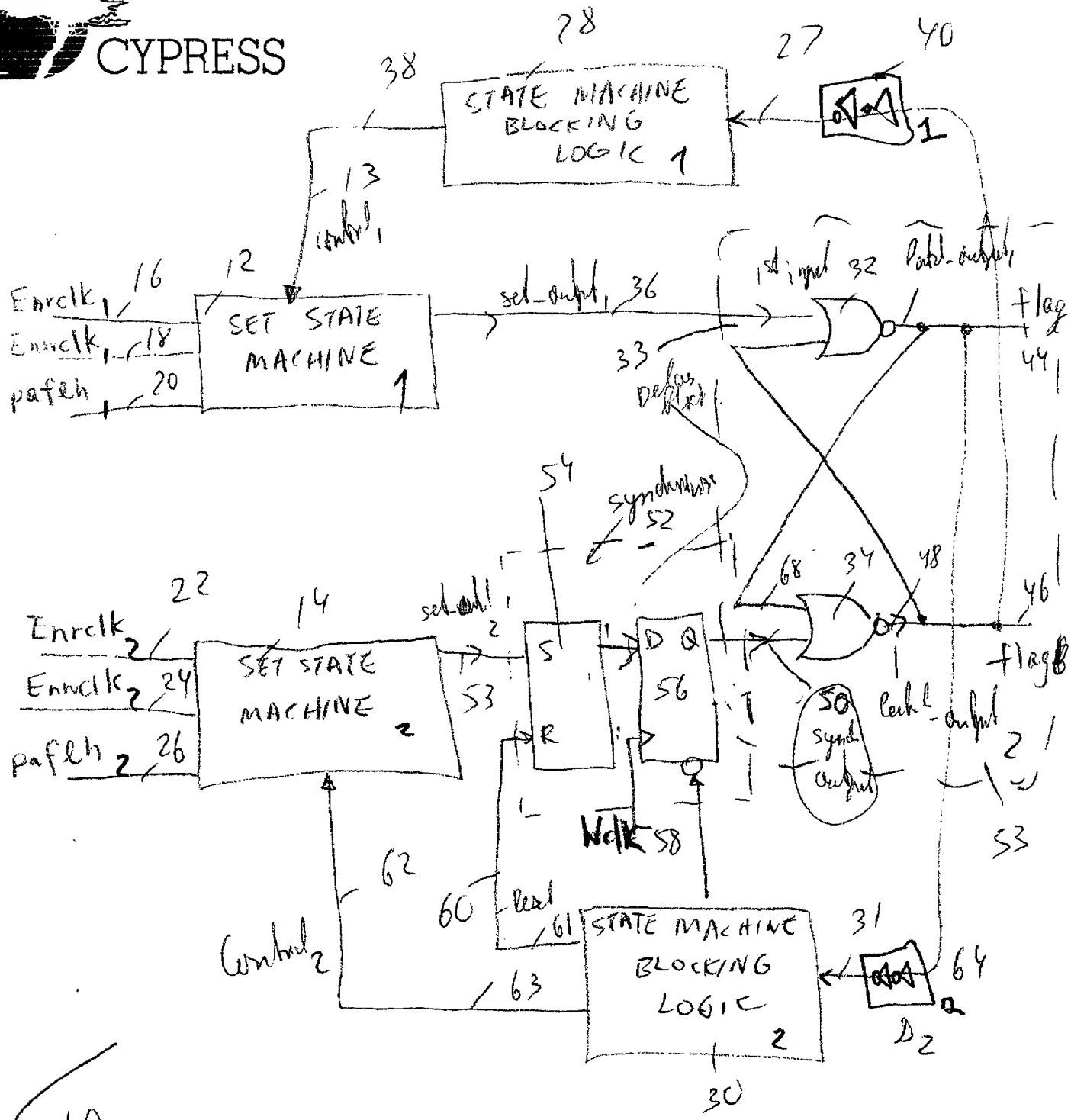

10

PAF → ~~rise and fall~~ Logic changes state only at rising edge of enabled write clock

FIG. 1

CYPRESS

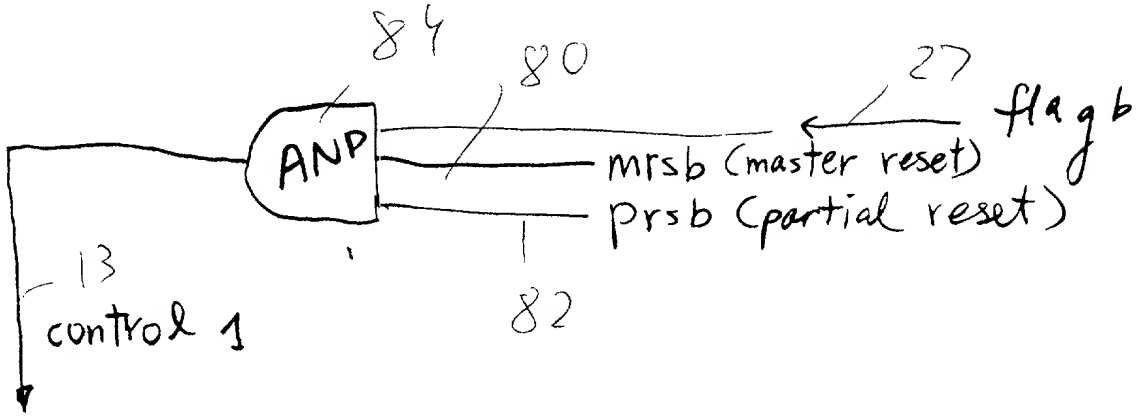

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FIG. 2A

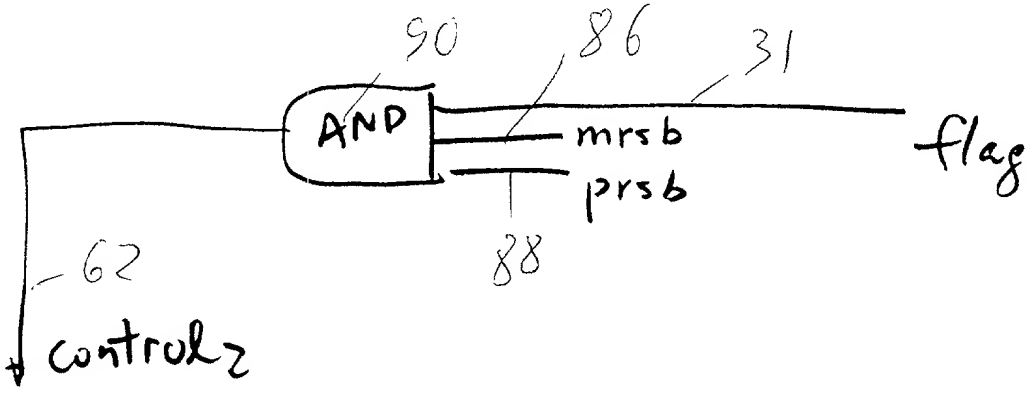

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FIG. 2B

PAE Blocking Logic

or PAF Blocking Logic

PAF

CYPRESS

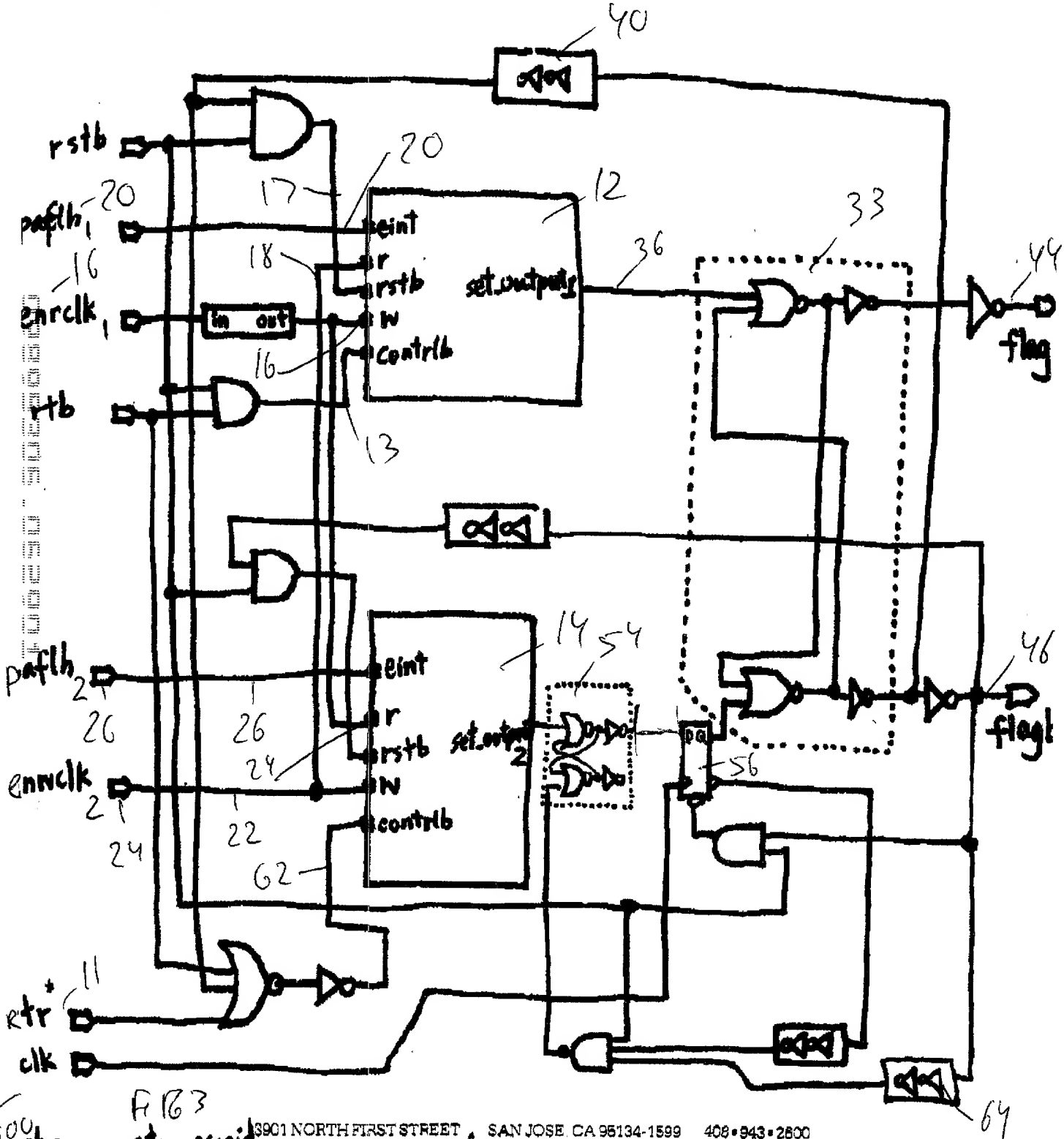

FIG 3

100 rtr — retransmit recovery signal

3901 NORTH FIRST STREET SAN JOSE CA 95134-1599 408•943•2600

CYPRESS

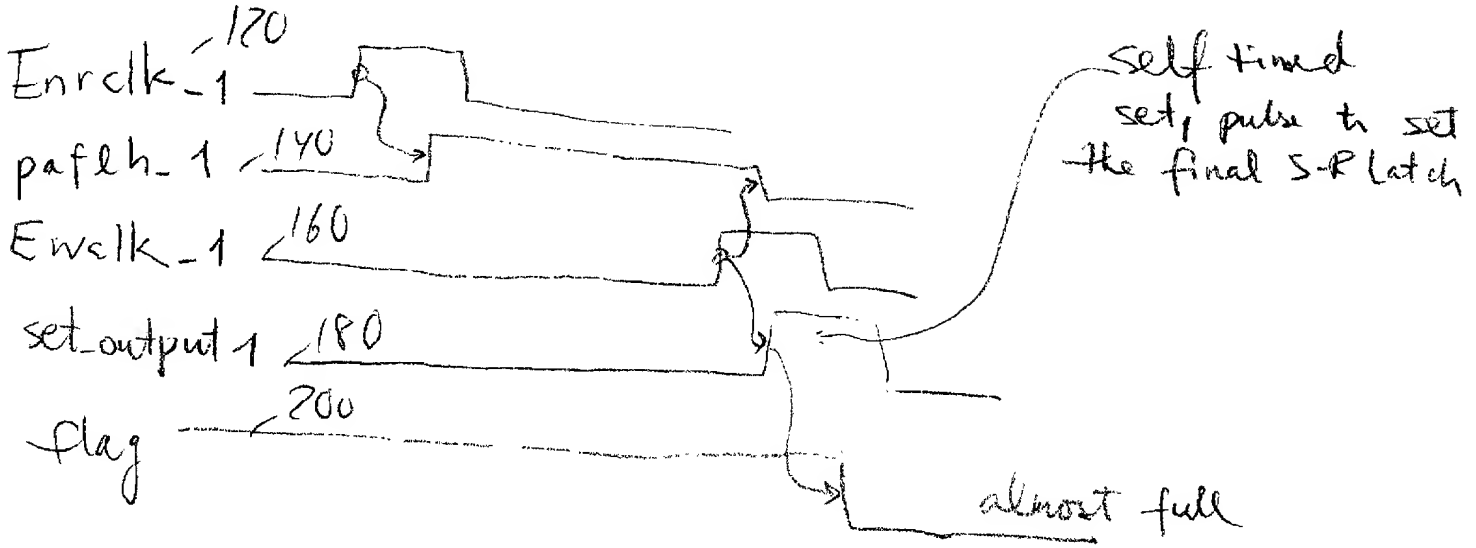

FIG. 4A

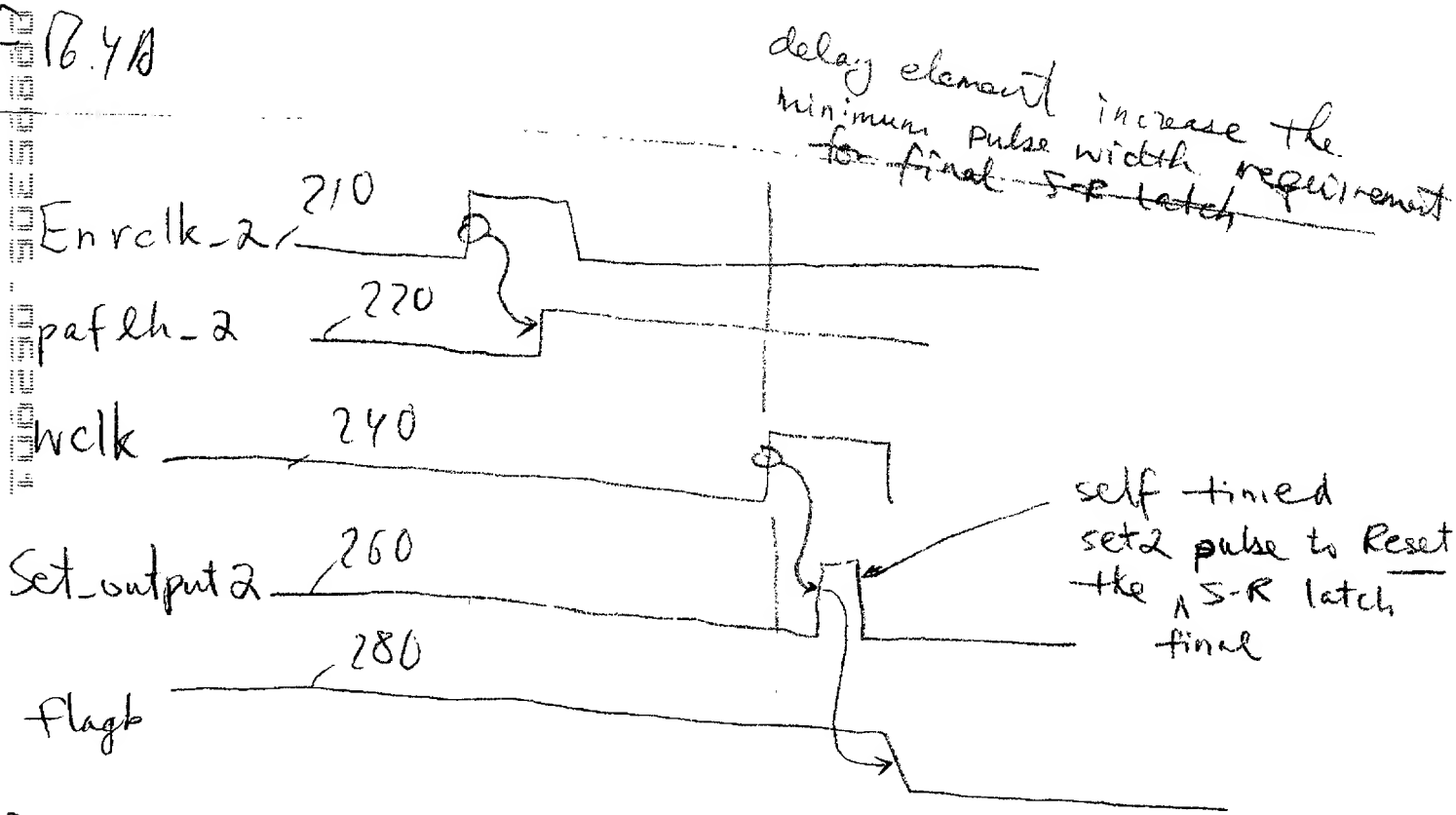

FIG. 4B

PAF

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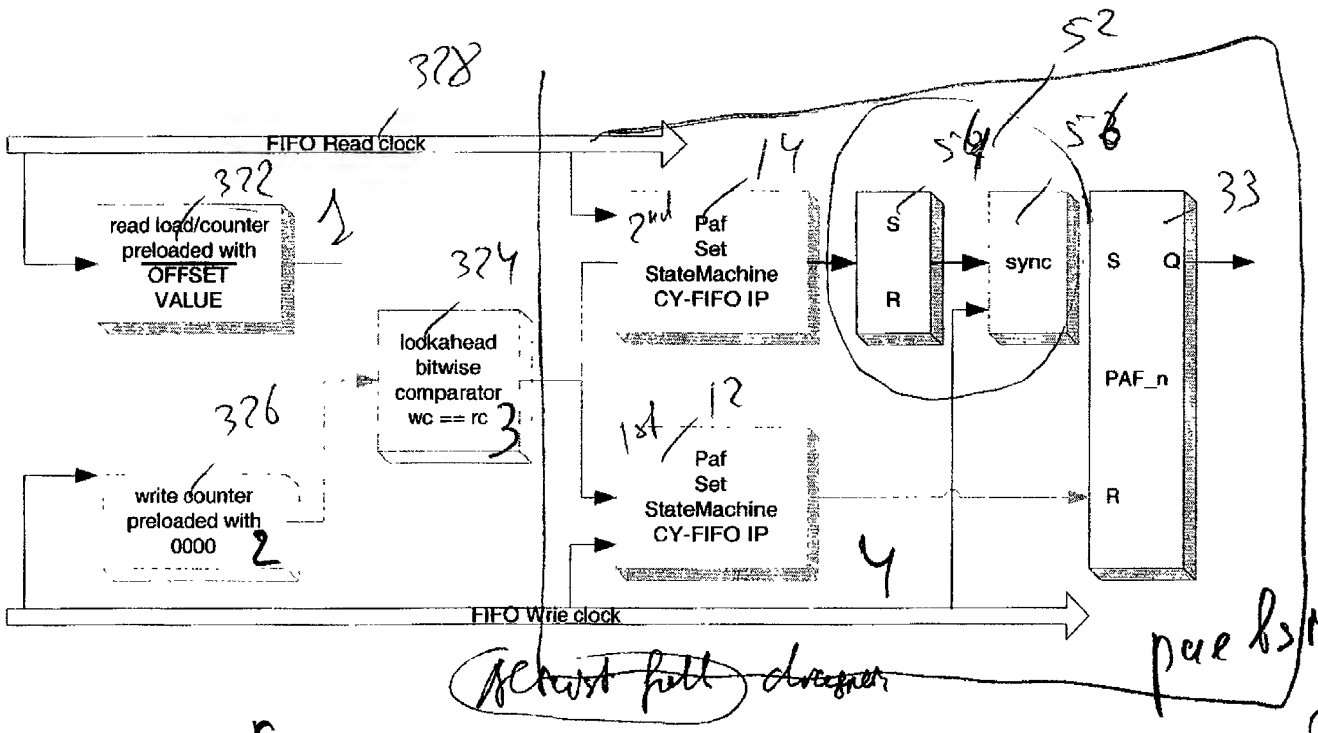
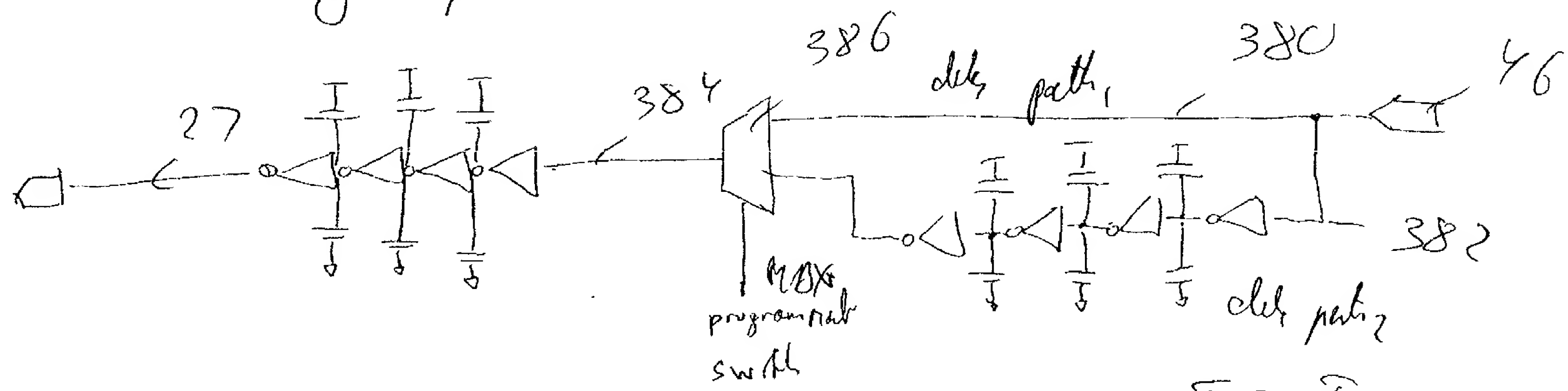
New block diagram



Architecture (Almost Full)

delay box/line



$\tau_2 > \tau_1$

P_2 & D_3 can be in different program.

40

FIG. 6

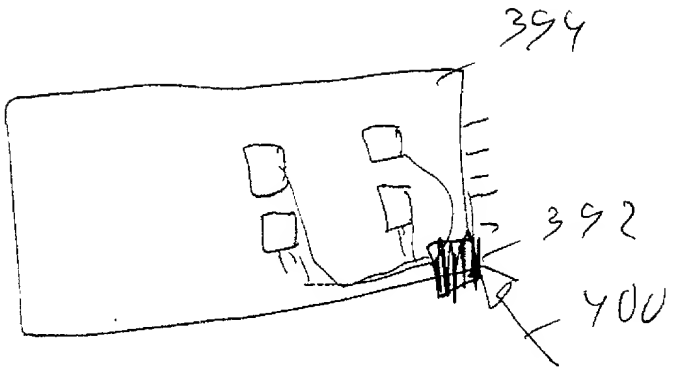


FIG 7A

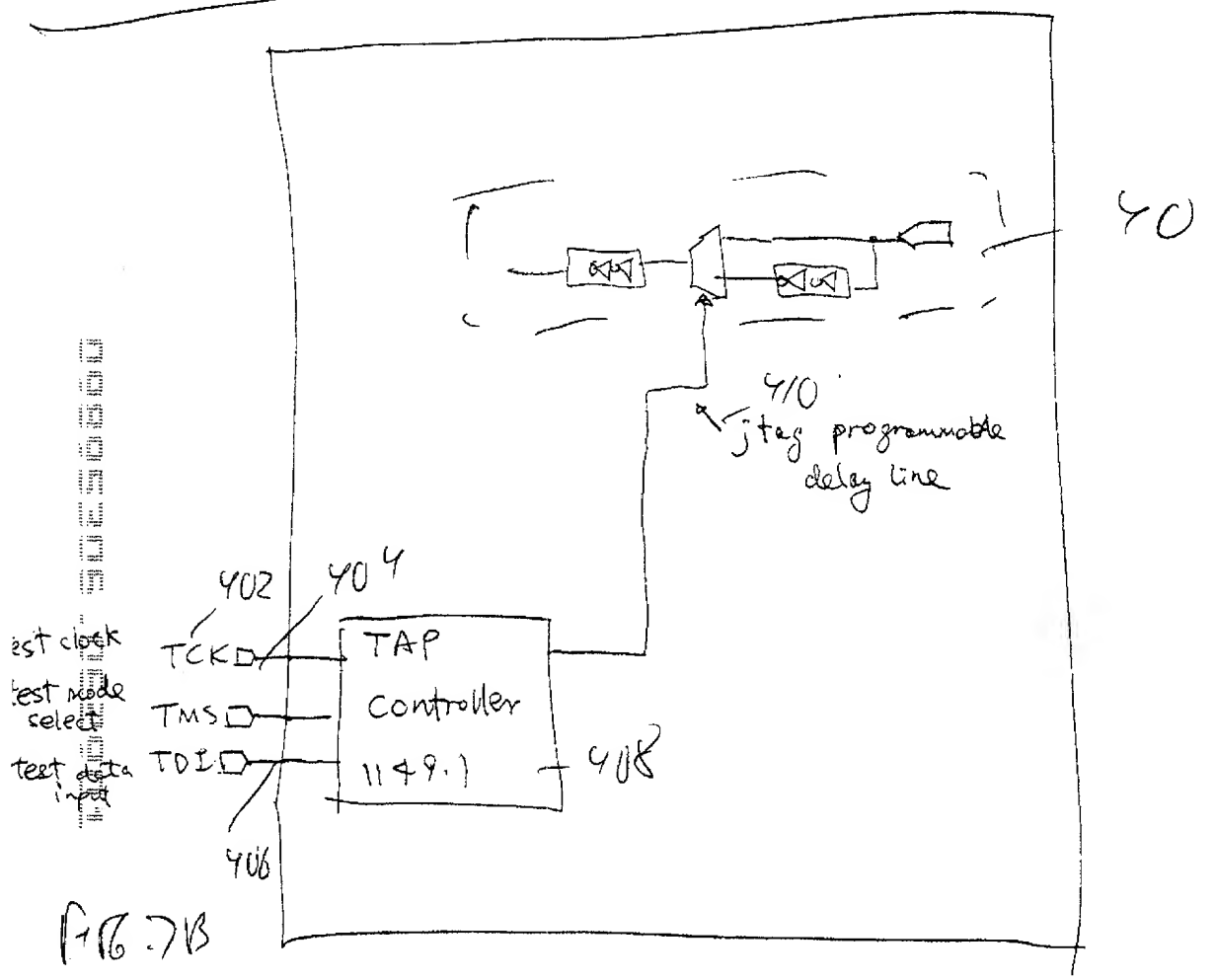


FIG. 7B

Benefits

- use existing jtag standard input pins
- just implement with an additional jtag instruction to program the delay line.